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A new interleaved high step up converter with low voltage stress on the main switches

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Abstract. In this paper, a new interleaved high step-up converter with low voltage stress on the switches is proposed. In the proposed converter, soft switching is provided for all switches by just one auxiliary switch, which decreases the conduction loss of auxiliary circuit. Also, the auxiliary circuit is expanded on the converter with more input branches. In the converter all main switches operate under zero voltage switching condition and auxiliary switch operate under zero current switching condition. Because of the interleaved structure, the reliability of converter increases and input current ripples decreases. The clamp capacitor in the converter not only absorb the voltage spikes across the switch due to leakage inductance, but also improve voltage gain. The proposed converter is fully analyzed and to verify the theoretical analysis, a 100 W prototype was implemented. Also, to show the effectiveness of auxiliary circuit on conduction EMI, EMI of the proposed converter comprised with hard switching counterpart.

Keywords: DC-DC converter; soft switching; electromagnetic interference; high step-up

1. Introduction

An important part in renewable energy systems is high step-up DC-DC converters, applied in interfacing cell to increase the low voltage of sources to required voltage level (Hwu and Peng 2015, Baharlou and Yazdani 2017). Examples of these applications are solar systems (Karthikeyan *et al.* 2019, Boussoula *et al.* 2020), hybrid vehicles systems (Divya Navamani *et al.* 2017, Van-Long *et al.* 2018), fuel cell systems (Pires *et al.* 2019, Bourada *et al.* 2019) and UPS (Alsolami *et al.* 2017). In these applications, the voltage difference between the two sides of the converter is high, therefore, the boost converters have to work with high duty cycle, which cause problems by increasing duty cycle. So, high step-up converters that can change the high voltage level with low duty cycle are importance. These converters should have high efficiency and low-cost, therefore, the use of non-isolated type is more appropriate (Zhao *et al.* 2011, 2019, Alsolami *et al.* 2018). In the isolated type (Meinagh *et al.* 2019, Yari *et al.* 2019, Santra *et al.* 2018, Abualnour *et al.* 2019, Belbachir *et al.* 2019, Medani *et al.* 2019, Sahla *et al.* 2019, Alimirzaei *et al.* 2019, Berghouti *et al.* 2019, Tlidji *et al.* 2019, Draoui *et al.* 2019, Rahmani *et al.* 2019, Boutaleb *et al.* 2019, Bousahla *et al.* 2020, Zarga *et al.* 2019) with the transformer ratio, the appropriate voltage gain can be achieved, but the use of transformer reduces efficiency and increases cost. An important parameter in high step-up converter is voltage stress across the switches. Decrease in the voltage stress of the switch cause to decrease conduction losses and converter cost. To reach this goal, the voltage gain of the converter should be increased. Many techniques have been introduced to increase voltage gain and decrease voltage stresses across the switches. These techniques can be divided to three main groups. The first technique is using of switched inductors and/or switched capacitors (Abbasi *et al.* 2019). The second group is voltage lifting technique (Liang *et al.* 2013). In this technique the capacitor charges in parallel way and discharges to the output in series. Finally, the third group is use of coupled inductor (Ebrahimi *et al.* 2019). The main drawbacks of this method are voltage spike due to leakage inductance of coupled inductor and pulsed current in the input side. To absorb the leakage inductance energy, clamp circuit should be used and to overcome pulsed input current, interleaved structure is proposed. In He *et al.* (2018) active clamp circuit is applied to the high step-up converter to absorb the leakage inductance energy and provide soft switching condition for all switches. But the number of switches increases and circulating current in auxiliary circuit is high which causes conduction losses. In Lin *et al.* (2014) a new high step-up is introduced, which by resonant technique, soft switching condition is provided. This converter has high efficiency and high voltage gain, but due to resonant condition in the circuit, current stress on the semiconductor devices are high and also the design and implementation of the control circuit of these converters is complex. In Meghdad *et al.* (2015) a new ZVS step-up converter is presented, which in this converter ZVS condition is provided for all switches, which cause high efficiency. This converter has high efficiency and low cost, but the voltage stress on the switch is high.

Regarding smart structures, static bending and strength

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behaviour of the laminated composite plate embedded with magnetostrictive (MS) material was computed numerically by Suman *et al*. (2017). Katariya *et al*. (2017) reported the thermal buckling strength of the sandwich shell panel structure and subsequent improvement of the same by embedding Shape Memory Alloy (SMA) fibre via a general higher-order mathematical model. A generic geometrical nonlinear mathematical model of smart composite curved shell panels was developed by Singh *et al*. (2018) for the evaluation of the linear and nonlinear dynamic responses. Biswas *et al*. (2018) discussed the detail design and development of an experimental test rig to derive usable energy by utilizing the waste heat energy through a heat exchanger made of Bi_2Te_3 material. experimental training of the commercial available Shape Memory Alloy (SMA) fibre under the combined thermomechanical loading was reported by Shinde *et al*. (2018).

Chaabane *et al.* (2019) presented static and dynamic behaviors of Functionally Graded Beams (FGB) is presented using a hyperbolic shear deformation theory. Boulefrakh *et al.* (2019) presented a simple quasi 3D hyperbolic shear deformation model for bending and dynamic behavior of Functionally Graded (FG) plates resting on visco-Pasternak foundations. Chaabane *et al*. (2019) studied free vibration of functionally graded plates on elastic foundations. Karami *et al*. (2019) studied size-dependent wave propagation analysis of FG anisotropic nanoplates based on a nonlocal strain gradient refined plate model. Boukhlif *et al*. (2019) studied a dynamic investigation of FG plates resting on elastic foundation using a simple quasi-3D higher shear deformation theory. Addou *et al*. (2019) investigated the effect of Winkler/ Pasternak/Kerr foundation and porosity on dynamic behavior of FG plates using a simple quasi-3D hyperbolic theory. Semmah *et al*. (2019) investigated the thermal buckling characteristics of zigzag Single-Walled Boron Nitride (SWBNNT) embedded in a one-parameter elastic medium. Mahmoudi *et al*. (2019) applied a refined quasi-three-dimensional shear deformation theory for thermo-mechanical analysis of functionally graded sandwich plates. Kaddari *et al*. (2020) studied structural behaviour of functionally graded porous plates on elastic foundation using a new quasi-3D model.

In this paper a new high step-up interleaved converter is proposed. In the proposed converter by using interleaved structure, the system reliability is increased and the input ripple is also reduced, which makes the converter suitable for applications such as solar systems cells and fuel cells systems. The proposed converter is analyzed and to confirm the theoretical analysis, the experimental results of the proposed converter are presented. Finally, the comparison between the proposed converter and hard switching converter is introduced, and also the comparison with other soft switching converters is presented.

2. Structure, operation and analysis

Structure of the proposed converter is shown in Fig 1. The proposed converter is an interleaved converter, which

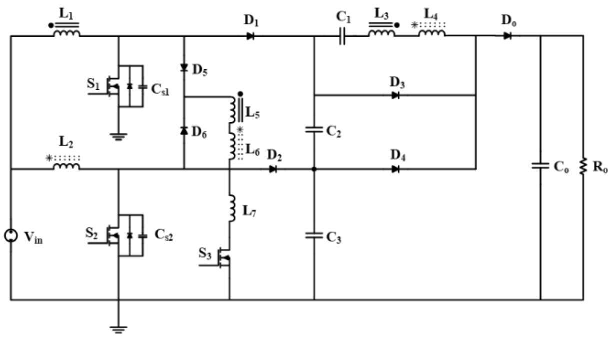

Fig. 1 Proposed converter structure

in this converter S_1 and S_2 are main switches of the interleaved converter. Interleaved structure is used to decrease input current ripple. In the proposed converter with a clamp passive circuit, the leakage inductances energy is absorbed, also these clamp capacitors contribute to increase voltage gain. S_3 is auxiliary switch, which turning on before main switches and providing soft switching condition for them. The auxiliary circuit consist of a switch with coupled inductors provides ZVS condition for main switches. The coupled inductors in the proposed converter cause to full discharge snubber capacitors on the main switches. On the other hand, the resonance inductor in the auxiliary circuit, in addition to discharge the snubber capacitors of the main switches, also provides ZCS condition for the auxiliary switch. As a result, the switching losses in the proposed converter improves significantly.

To increase voltage gain and decrease voltage stress, coupled inductors and series capacitor technique have been used. Finally, the increasing phases in the proposed converter is simple, which can be increased the number of parallel phases without limitation and only uses an auxiliary circuit to provide soft switching condition for all switches.

To simplify analysis of the proposed converter several assumptions are considered as below (Fig. 1):

- All semiconductors are ideal.
- C_O is large enough, so voltage at output is fixed in one switching cycle.
- The inductances at input (L_1, L_2) are large enough, so the current of these inductances are fixed in one switching cycle.
- C_1, C_2 and C_3 are large and voltage of these capacitors are fixed.

The proposed converter has 8 modes at one switching cycle. Before mode 1, S_2 and S_1 are off, D_3 and D_4 conduct and D_O is off. The key waveform of the proposed converter is shown in Fig. 2.

Mode 1 (t_0-t_1): Before turning on S_1, the auxiliary switch (S_a) turns on to discharge the snubber capacitor of S_1. Therefore, this mode begins by turning on of S_a. due to existence of L_7, this switch is turned on under ZCS condition. L_a starts to resonant with C_{S1}, which cause to discharge C_{S1}. In this mode all diodes are off except D_a. This mode ends when C_{S1} is fully discharged.

$$i_{CS1} = \frac{V_o}{Z} sin\omega_r (t - t_0) \tag{1}$$

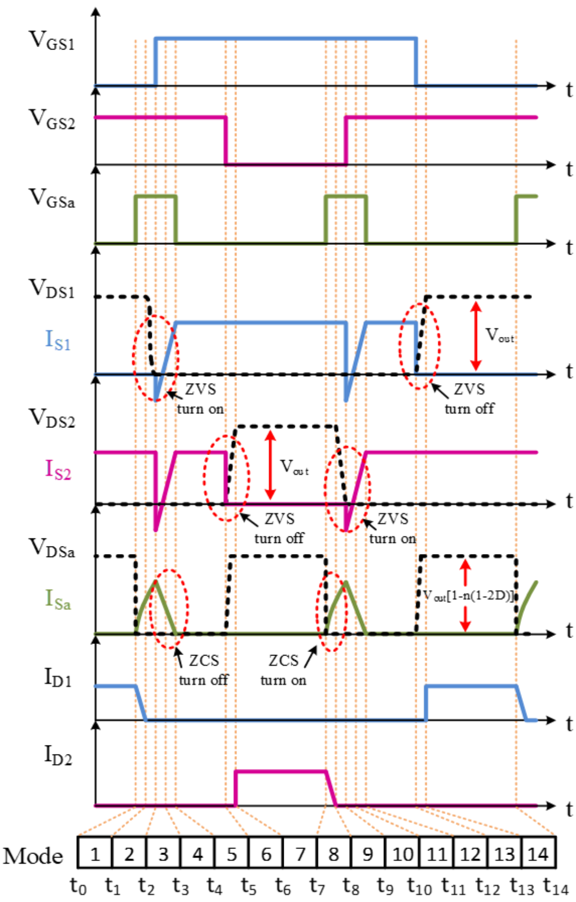

Fig. 2 The key waveform of the proposed converter

$$V_{CS1} = V_{S1} = V_O cos\omega_r(t - t_0) - V_O \tag{2}$$

$$Z = \sqrt{\frac{L_7}{C_{S1}}} \tag{3}$$

$$\omega_r = \frac{1}{\sqrt{L_7 C_{S1}}} \tag{4}$$

Mode 2 (t_1-t_2): With full discharge C_{S1}, the body diode of this switch conducts and from this instant S_1 can be turned on under ZVS condition. In this mode a fixed voltage (V_1) drops across L_a inversely, and its current decreases Linearly. In this mode the body diodes of S_1 and S_2 conducts until the current of the auxiliary switch is zero and turns off under ZCS condition.

$$I_{L7} = -\frac{V_1}{L_7}(t - t_1) + I_{L7}(t_1) \tag{5}$$

$$I_{S1} = \frac{V_1}{L_7}(t - t_1) + I_{S1}(t_1) \tag{6}$$

Mode 3 (t_2-t_3): This mode begins when S_a is turned off and since the currents of S_1 and S_2 are established, the magnetic inductances (L_{m1} and L_{m2}) are charged and the load current is supplied by the output capacitor.

Mode 4 (t_3-t_4): In this mode S_2 is turned off and D_2 conducts immediately, which L_{K2} energy is discharged into the clamp capacitor (C_3). On the other hand, the output diode turns on to discharge the magnetizing inductor (L_{m2}) at the output. This mode ends when the auxiliary switch is turned on.

Mode 5 (t_4-t_5): By turning on S_a, L_a starts to resonant with C_{S2} and discharge it resonantly. This mode ends when C_{S1} is fully discharge. The equations for this resonant is shown below.

$$i_{CS2} = \frac{V_o}{Z} sin\omega_r(t - t_4) \tag{7}$$

$$V_{CS2} = V_{S2} = V_O cos\omega_r(t - t_4) - V_O \tag{8}$$

$$Z = \sqrt{\frac{L_7}{C_{S2}}} \tag{9}$$

$$\omega_r = \frac{1}{\sqrt{L_7 C_{S2}}} \tag{10}$$

Mode 6 (t_5-t_6): In this mode the body diodes of S_1 and S_2 conduct and the current of L_a is decreased linearly. In this mode S_2 can be turned on under ZVS condition. As the current increases, the switch current is transferred from the body diode to the switch and increases with the same slope until the auxiliary switch current is zero and this mode ends.

$$I_{L7} = I_{S3} = -\frac{2NV_{in}}{L_7}(t - t_5) + I_{L7}(t_5) \tag{11}$$

Mode 7 (t_6-t_7): When the current of auxiliary switch reach to zero, both magnetic inductors (L_{m1} and L_{m2}) start charging and all diodes are off until S_1 is turned off.

Mode 8 (t_7-t_8): At t_7, S_1 is turned off and D_1 conducts immediately to transfer leakage inductance energy to C_1. Also, D_3 and D_4 conducts to transfer clamp capacitor energy to C_L, which this condition increases the voltage gain in the proposed converter.

The equivalent of these modes is shown in Fig. 3.

3. Structure, operation and analysis II

$$N_1 = \frac{n_3}{n_1} \tag{12}$$

$$N_2 = \frac{n_5}{n_1} \tag{13}$$

$$N_3 = \frac{n_4}{n_2} \tag{14}$$

$$N_4 = \frac{n_6}{n_2} \tag{15}$$

where n_3 is number L_3 round, n_1 is number L_1 round, n_5 is number L_5 round, n_4 is number L_4 round and n_6 is number L_6

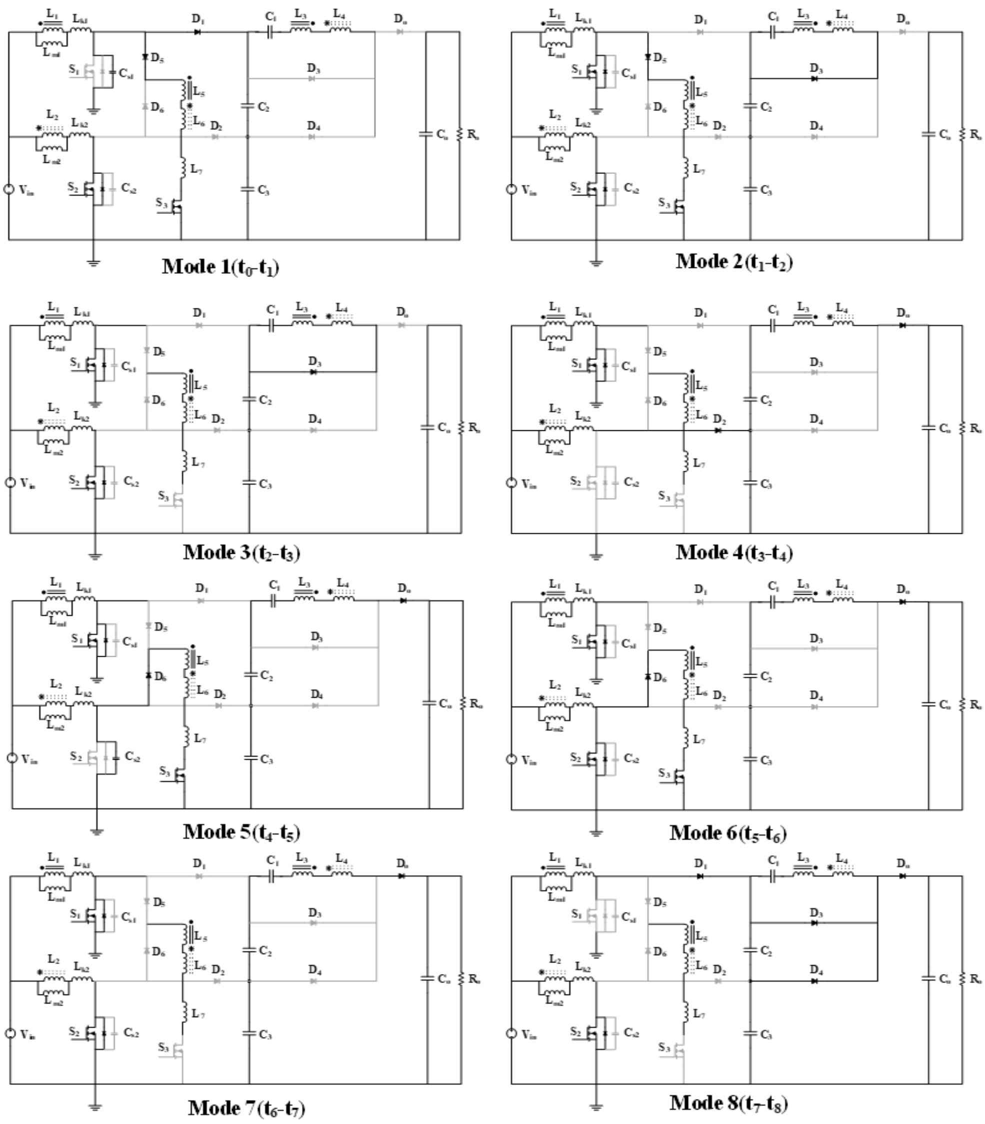

Fig. 3 The equivalent circuits of the proposed converter

round.

To simplify the design of the elements, these ratios are assumed to be equal to *N*.

3.1 Voltage gain

To calculate voltage gain of the proposed converter, the voltage of C_2 and C_3 should be calculated.

$$V_{in}DT = (V_{C2} - V_{in})(1-D)T \tag{16}$$

$$V_{C2} = \frac{V_{in}}{1-D} \tag{17}$$

$$V_{in}DT = (V_{C3} - V_{in})(1-D)T \tag{18}$$

$$V_{C3} = \frac{V_{in}}{1-D} \tag{19}$$

When S_1 is off and D_3 conducts, V_{C1} is calculated by writing KVL in the loop.

$$KN(V_{C2} - V_{in}) + KNV_{in} - V_{c3} = 0 \tag{20}$$

$$V_{C1} = KN\frac{V_{in}}{1-D} \tag{21}$$

where *K* is the coupling factor of the coupled inductors.

When S_1 is off and D_1 conducts, voltage gain can be calculated from equation below.

$$-V_{in} - K(V_{C2} - V_{in}) - V_{C1} - KNV_{in} - KN(V_{C1} - V_{in}) + V_O = 0 \tag{22}$$

$$\frac{V_O}{V_{in}} = \frac{2 + 2KN + (K-1)D}{1-D} \tag{23}$$

According to Eq. (23), Fig. 4 is plotted. As can be seen, the voltage gain increases by increasing turns ratio of the coupled inductors, but it causes to increase ohmic losses of windings and leakage inductance of the coupled inductor. In this figure *K* assumed to be fixed and equal to 0.99.

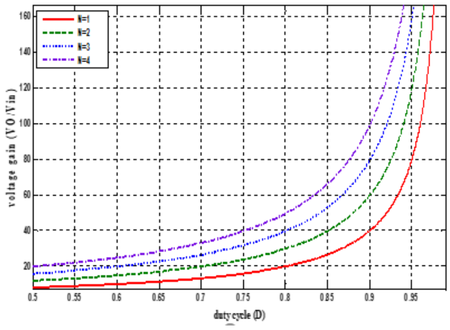

Fig. 4 Voltage gain of the proposed converter versus duty cycle in different turns ratio

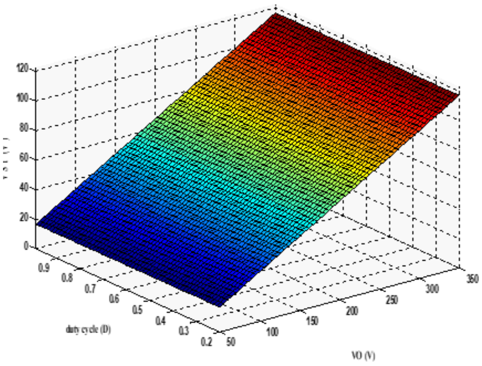

Fig. 5 Voltage stress on main switch according to D and V_O

3.2 Voltage stress of semiconductor devices

S_1 and S_2 voltages are clamped to the voltage levels of C_2 and C_3. Hence the voltage stress of these switches is equal to

$$V_{S1} = V_{S2} = \frac{V_{in}}{1-D} = \frac{V_O}{2+2KN+(K-1)D} \tag{24}$$

Fig. 5 shows the voltage stress on the main switch versus N and D, which illustrates the effectiveness of the proposed circuit to decrease voltage stress with basic.

$$V_{D1} = V_{C2} + V_{C3} = \frac{2V_O}{2+2KN+(K-1)D} \tag{25}$$

$$V_{D2} = V_{C3} = \frac{V_O}{2+2KN+(K-1)D} \tag{26}$$

When S_2 is off, voltage stress of D_3 can be obtained as below

$$-V_{in} - K(V_{C2} - V_{in}) - V_{C2} - V_{D3} + V_O = 0 \tag{27}$$

$$V_{D3} = \frac{2KN}{2+2KN+(K-1)D} V_O \tag{28}$$

$$V_{D4} = V_{DO} = V_O - \frac{V_{in}}{1-D} = \frac{1+2KN+(K-1)D}{2+2KN+(K-1)D} V_O \tag{29}$$

$$V_{D5} = V_{L5} + V_{L6} \tag{30}$$

where V_{L5} and V_{L6} are voltage across L_5 and L_6 in mode 5, which are calculated from below.

$$V_{L5} = \frac{1}{N} V_{in} - (1+N)(V_O - V_{C1} - V_{C2} - V_{C3}) \tag{31}$$

$$V_{L6} = N(V_O - V_{C1} - V_{C2} - V_{C3}) \tag{32}$$

$$V_{D5} = \frac{1}{N} V_{in} - (V_O - V_{C1} - V_{C2} - V_{C3})(1-N)(-N) \tag{33}$$

Also, according to the modes of the proposed converter, the voltage stress of the D_6 and D_5 are similar.

$$V_{D6} = \frac{1}{N} V_{in} - (V_O - V_{C1} - V_{C2} - V_{C3})(1-N)(-N) \tag{34}$$

3.3 Design of the inductors

To calculate of the inductors, the second balance current is written

$$(1-A)I_{Lm1}(1-D)T = \frac{I_{Lm2}}{2}(1-D)T \tag{35}$$

where A is a constant number, which is the coefficient of current on the L_{m1} at the specified time.

$$I_{Lm2} = 2(1-A)I_{Lm1} \tag{36}$$

$$AI_{Lm1}(1-D)T = \frac{I_{Lm2}}{2}(1-D)T \tag{37}$$

$$I_{Lm2} = 2AI_{Lm1} \tag{38}$$

A should be calculated, which is obtained by equalizing Eqs. (25) and (27).

$$2AI_{Lm1} = 2(1-A)I_{Lm1} \tag{39}$$

As a result

$$A = \frac{1}{2} \tag{40}$$

which this result shows that I_{Lm1} is equal to I_{Lm2}

$$I_{Lm1} = I_{Lm2} \tag{41}$$

$$I_{in} = I_{Lm1} + I_{Lm2} \tag{42}$$

$$I_{in} = 2I_{Lm1} \tag{43}$$

assuming one hundred percent efficiency, and the relationship of inductor, inductor value is calculated as below.

$$P_{in} = P_{out} \tag{44}$$

$$V_{in}I_{in} = V_{out}I_{out} \tag{45}$$

$$I_{Lm1} = I_{Lm2} = \frac{2}{1-D} I_{out} \tag{46}$$

$$V_L = L\frac{\Delta_{IL}}{\Delta_t} \tag{47}$$

$$L_{m1} = L_{m2} = \frac{V_{in}D}{\Delta_{ILm}f} \tag{48}$$

3.4 Design of the capacitors

By using charge and discharge current of the capacitors, the value of them can be calculated as below

$$\frac{I_{Lm2}}{2}(1-D)T = C\Delta_{VC} \tag{49}$$

$$C_1 = C_2 = \frac{I_{out}}{f\Delta_{VC}} \tag{50}$$

where Δ_{VC} is voltage ripple in C_1 or C_2 and usually selected as $0.1V_C$

$$I_{out}(1-D)T = C_O\Delta_{VCO} \tag{51}$$

$$C_O = \frac{I_{out}(1-D)}{f\Delta_{VCO}} \tag{52}$$

$$\frac{1}{2}L_{lk}I_{Lm2}^2 = C_2\Delta_{VC2} \tag{53}$$

$$C_3 = \frac{L_{lk2}I_{Lm}^2}{2\Delta_{VC3}} \tag{54}$$

4. Experimental results

To verify the theoretical analysis, a 100 W prototype of the proposed converter is implemented and tested, which the values of the elements are shown in Table 1. The photo of the prototype of the proposed converter is shown in Fig. 6. The experimental results of the voltage and current of the semiconductor devices are shown in Fig. 7.

As can be seen that the experimental results are verified the theoretical analysis. In Figs. 7(a) and (b) the current of S_1 and S_2 in turning on instant is negative, which shows the body diode of the switch conducts and ZVS condition is provided. For S_3 the current is increased and decreased with slope, which shows ZCS condition is established. For all diodes in Fig. 7, it is evident that the current decreases and increases with the slope, which is shown ZCS condition is provided for theses diodes.

The proposed converter is tested for EMI noise based on CISPR22 standard, and the result of the test is shown in Fig. 8. Also, a sample of the hard-switching counterpart is tested to compare with the proposed converter and the result is shown in Fig. 9. According to the measured spectrum it is clear that the noise amplitude in the proposed converter is decreased, which an improvement about 10 dB/μv is observed.

Table 1 Value of the elements in the proposed converter

Parameter or element	Value
V_{in}	24 V
V_O	340 V
S_1, S_2, S_3	IRF740
D_1, D_2, D_3, D_4, D_5, D_6, D_O	MUR860
L_{m1}, L_{m2}	400 μH
$N_1 = N_2 = N_3 = N_4 = N$	2
L_7	40 μH
C_1, C_2, C_3	10 μF
P_O	100 W
f_{SW}	100 kHZ
C_O	100 μF

Fig. 6 The photo of the prototype of the proposed converter

5. Comparison between the proposed converter with other converters

The proposed converter efficiency is compared with the hard-switching high step-up conventional converter with same structure these results are shown in Fig. 10, which the results show that the efficiency has improved 6% over the hard-switching counterpart at full load.

The proposed converter is compared with three soft switching converter and the results are presented in Table 2. Converter in Eq. (20) has low number of switches, but this converter has a high number of capacitor and a relatively low voltage gain. Converter in Eq. (21) has better voltage gain, but the number of diodes is high and has low efficiency because of high circulating current. The problem in converters Eqs. (22) and (24) is the use of two switches in their auxiliary circuit, which complicates the control of this converter. Converter in Eq. (23) has high voltage gain and only has two switches, but this converter has three coupled inductors that cause to increasing cost and value of the converter.

Fig. 11 shows the comparison between proposed converter with five soft switching converter according to

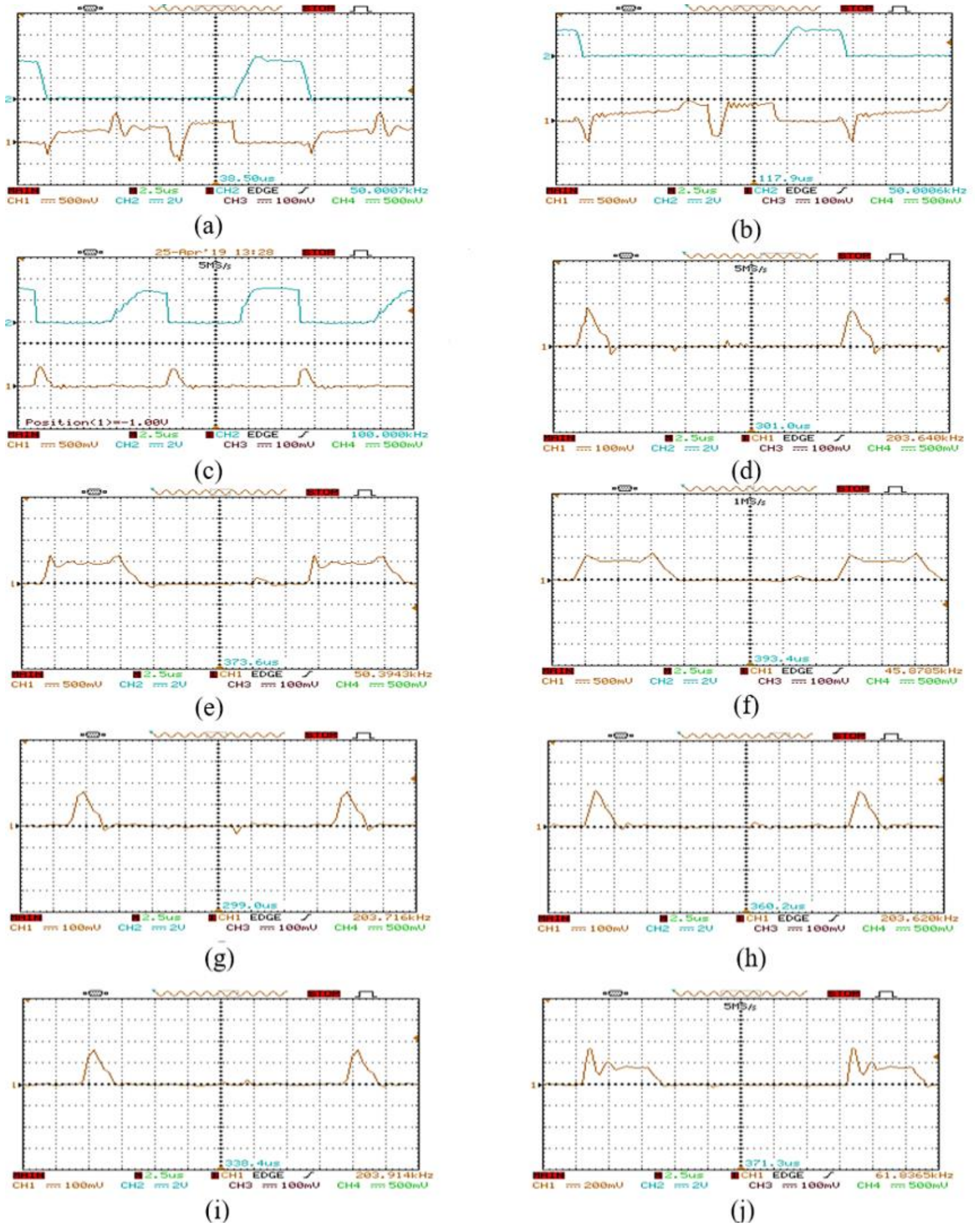

Fig. 7 The experimental results of the voltage and current of the semiconductor devices: Voltage (up) and current (down) of (a) S_1, (b) S_2, (c) S_3 (vertical scale 100 volt/div or 0.5 A/div, horizontal scale 1 μs/div); current of (d) D_1, (e) D_2, (f) D_3, (g) D_4, (h) D_5, (i) D_6, (j) D_0 (vertical scale 0.5 A/div) (for all shapes horizontal scale is 1 μs/div)

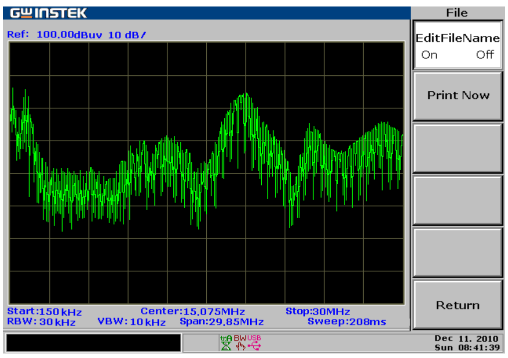

Fig. 8 The experimental results of the EMI test in proposed converter

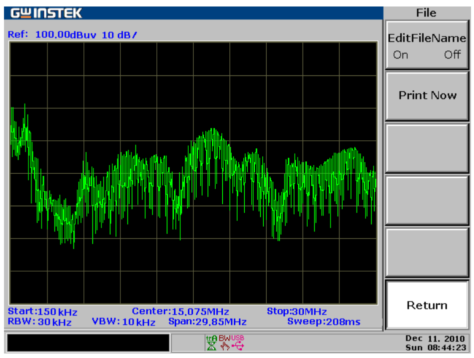

Fig. 9 The experimental results of the EMI test in hard switching converter

Table 2 Comparison results between the proposed converter with other converters

Topology	Nouri *et al*. (2014)	Packnezhad *et al.* (2019)	He *et al.* (2019)	Nouri *et al*. (2019)	Nouri *et al*. (2017)	Proposed converter
Number of switches	2	3	4	2	4	3
Number of diodes	6	10	6	6	6	7
Number of capacitor	5	6	9	5	7	3
Number of coupled inductors	2	3	2	3	2	2
Voltage gain	$\frac{3N+1}{(1-D)\left[1+\left(\left(L_{LK2}f_s(3N+1)^2\right)/\left(2R_O(1-D)^2\right)\right)\right]}$	$\frac{1+3n}{1-D}$	$\frac{2(1+N)}{1-D}$	$\frac{2(N+1)+n}{1-D}$	$\frac{1+6N}{1-D}$	$\frac{2+2KN+(K-1)D}{1-D}$
Voltage stress on main switch	$\frac{V_O}{3N+1}$	$\frac{V_O}{1+3n}$	$\frac{V_{in}}{1-D}$	$\frac{V_O}{2(N+1)+n}$	$\frac{V_O}{6N+1}$	$\frac{V_O}{2+2KN+(K-1)D}$
Efficiency	95%	95%	96%	95%	94%	95.5%

Table 3 Losses analysis in the proposed converter and hard switching converter

Losses	Formula	Hard switching converter	Proposed converter
Switching loss in S_1	$\left[\frac{1}{2}V_{DS1}I_{S1}\left(t_{on}+t_{off}\right)+V_{DS1}t_{rr}(I_{S1}+I_{rr})\right]f_{SW}$	6.35 W	zero
Switching loss in S_2	$\left[\frac{1}{2}V_{DS2}I_{S2}\left(t_{on}+t_{off}\right)+V_{DS2}t_{rr}(I_{S2}+I_{rr})\right]f_{SW}$	6.35 W	zero
Switching loss in S_3	$\left[\frac{1}{2}V_{DS3}I_{S3}\left(t_{on}+t_{off}\right)+V_{DS3}t_{rr}(I_{S3}+I_{rr})\right]f_{SW}$	zero	zero
Conduction loss in S_1	$I_{S1(rms)}^2R_{ds1}$	0.6 W	0.6 W
Conduction loss in S_2	$I_{S2(rms)}^2R_{ds2}$	0.6 W	0.6 W
Conduction loss in S_3	$I_{S3(rms)}^2R_{ds3}$	zero	0.4 W
Conduction loss in D_1	$V_{F(D1)}I_{F(D1-ave)}$	zero	0.11 W
Conduction loss in D_2	$V_{F(D2)}I_{F(D2-ave)}$	zero	0.15 W
Conduction loss in D_3	$V_{F(D3)}I_{F(D3-ave)}$	zero	0.23 W
Conduction loss in D_4	$V_{F(D4)}I_{F(D4-ave)}$	zero	0.135 W
Conduction loss in D_5	$V_{F(D5)}I_{F(D5-ave)}$	zero	0.1265 W
Conduction loss in D_6	$V_{F(D6)}I_{F(D6-ave)}$	zero	0.11 W
Conduction loss in D_O	$V_{F(Do)}I_{F(Do-ave)}$	1 W	0.8 W
Parasitic capacitance loss in S_1	$\frac{1}{2}C_{par}V_{DS1}^2f_{SW}$	1.2 W	0.27 W
Parasitic capacitance loss in S_2	$\frac{1}{2}C_{par}V_{DS2}^2f_{SW}$	1.2 W	0.28 W
Parasitic capacitance loss in S_3	$\frac{1}{2}C_{par}V_{DS3}^2f_{SW}$	zero	0.25 W
Total losses	-------	17.3 W	4.1 W

voltage gain. in this figure it is clear that the converter has the highest gain, but this converter has high number of elements., also this converter has low efficiency.

Fig. 12 shows the comparison between proposed converter with other soft switching converter according to voltage stress on the main switch. In this figure, V_O assumed fix and equal to 320 volts. As can be seen from this figure, voltage stress by increasing of N decreases and for proposed converter, voltage stress lower than other converters.

For the proposed converter, based on the losses on the elements, the analysis is performed and the results of this analysis are presented in Table 3. Also, for comparison in this table a hard-switching converter is analysis and results are presented. As can be seen, the proposed converter losses less than hard switching converter, therefore the efficiency

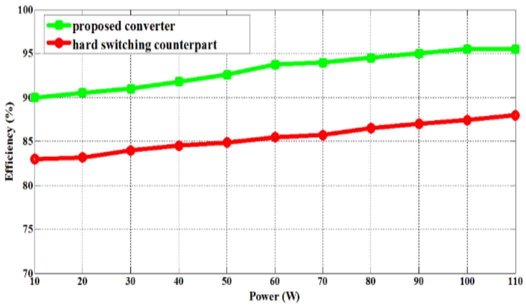

Fig. 10 The efficiency of the proposed converter with comparison to the hard-switching converter

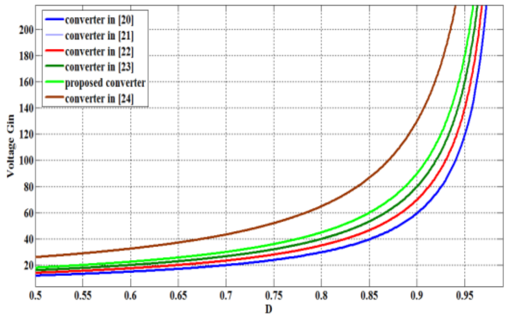

Fig. 11 Comparison between proposed converter with other soft switching converter according to voltage gain

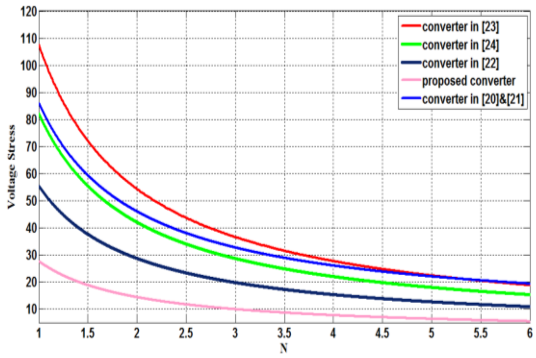

Fig. 12 Comparison between proposed converter with other soft switching converter according to voltage stress

of the converter is theoretically high.

Table 3 shows the loss analysis in the proposed converter, which this analysis compared with hard switching converter in this table.

6. Conclusions

In this paper a new soft switching high step-up interleaved converter is proposed. The proposed converter has high voltage gain and low voltage stress on the switches. Due to interleaved technique, the proposed converter has high reliability and low input current ripple. The proposed converter phases are easily expandable and no new auxiliary circuit is needed. By using coupled inductors, voltage gain increases and input current ripple decreases. In the proposed converter, by using a clamp circuit, the voltage stress on the switches is reduced relative to the output voltage. Also, this clamp circuit absorbs the leakage inductors energy and prevents spikes on the switch. The proposed converter has been analyzed and to verify theoretical analysis, the experimental results are presented.

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