Advances in Nano Research, *Vol. 5, No. 1 (2017) 61-67*
DOI: https://doi.org/10.12989/anr.2017.5.1.061

An approach to model the temperature effects on I-V characteristics of CNTFETs

Roberto Marani [1a] and Anna G. Perri [*2]

[1] *Consiglio Nazionale delle Ricerche, Istituto di Studi sui Sistemi Intelligenti per l'Automazione, Bari, Italy*
[2] *Dipartimento di Ingegneria Elettrica e dell'Informazione, Laboratorio di Dispositivi Elettronici, Politecnico di Bari, Italy*

(*Received November 10, 2016, Revised January 17, 2017, Accepted January 19, 2017*)

Abstract. A semi-empirical approach to model the temperature effects on I-V characteristics of Carbon Nanotube Field Effect Transistors (CNTFETs) is proposed. The model includes two thermal parameters describing CNTFET behaviour in terms of saturation drain current and threshold voltage, whose values are extracted from the simulated and trans-characteristics of the device in different temperature conditions. Our results are compared with those of a numerical model online available, obtaining I-V characteristics comparable but with a lower CPU calculation time.

Keywords: nanoelectronic devices; carbon nanotube field effect transistors; modeling; device simulation; I-V characteristics; temperature effects; computer aided design

1. Introduction

Carbon NanoTubes have attracted much interest in the scientific world due to their excellent electrical, thermal, and mechanical properties. In particular CNTFETs, which are field-effect transistors that utilize a single carbon nanotube or an array of carbon nanotube as the channel material instead of bulk silicon in the traditional MOSFET structure, are now a promise for an alternative material to replace silicon in future electronics (Avouris *et al*. 2005, Marani and Perri 2009, 2011, 2012, Gelao *et al*. 2011, Marani *et al*. 2012, 2013, Gelao *et al*. 2015a, b).

As prediction through modeling forms the basis of engineering design, engineers need models which relate to their design area and are adaptable to new design concepts.

Most of the CNTFET models available in literature are numerical and make use of self-consistency and therefore they cannot be directly implemented in modeling languages for analog and digital circuits, such as SPICE, Verilog or VHDL-AMS. Moreover the research on temperature effects on DC characteristics of CNTFETs is still at an early stage.

Generally there are two methods for developing thermal models of electronic devices (Perri 2011, Marani and Perri 2012).

The first method consists of the calculations of the thermal gradient inside the device and drain-source current I_{ds}, since the thermal field depends on the consumed power. This procedure allows

*Corresponding author, Professor, E-mail: annagina.perri@poliba.it
[a] Ph.D., E-mail: marani@ba.issia.cnr.it

 ISSN: 2287-237X (Print), 2287-2388 (Online)

good agreement between the measured and simulated I-V static characteristics at different temperatures but it results rather heavy from a computational point of view. On the other hand, physical models of the temperature dependence of device parameters must take into account a number of physical factors, such as, for example, the energy gap, the available state density at the conducting and valence band edge, the dielectric constant, the electron saturation velocity, the electron mobility (Perri 2011). Therefore the approach generally used for the thermal modeling lies in accounting for the device parameter dependence as linear or non linear functions of temperature. In these functions temperature coefficients, depending on the device technology and bias voltages, are used. Physical modeling of bias dependence on the device characteristics can be accurate enough if analytic expressions take into account a lot of second order effects, such as the negative output conductance, especially due to self-heating. Thus model expressions become very complicated. This makes it very difficult to model the large signal behavior by means of physical expressions and to derive an analytic small signal model from the large signal one. On the other hand, physical models do not require an electrical characterization of the devices.

The second method is based on a semi-empirical approach, where some of the fitting parameters of the large signal model are dependent on the temperature according to empirical relationships including fitting parameters having a physical meaning. However the semi-empirical model requires the electrical characterization of devices and the delicate procedure of parameters extraction.

In this paper we have followed this second approach, because it can be considered more useful for computer-aided design (CAD) applications, since it is less complicated without any loss of accuracy, can be easily implemented in an electrical simulator and the computational time is very low. In particular we have firstly enhanced a semi-empirical model, already proposed by us (Marani and Perri 2012), to simulate very accurately the effect of device negative output conductance, especially due to self-heating. Then the temperature effects on I-V characteristics have been modeled by the dependence on temperature of the device threshold voltage and of the maximum saturation drain-source current, whose values have been extracted from the simulated and trans-characteristics of the device in different temperature conditions.

Moreover, in order to validate our results, they have been also compared with data obtained from simulator online available (Rahman *et al*. 2006), obtaining I-V characteristics comparable but with a lower CPU calculation time.

The presentation is organized as follows. The proposed model is presented in Section 2, while the discussion of simulation results is given in Section 3. The conclusions and future developments are described in Section 4.

2. The proposed thermal I-V model of CNTFETs

In Marani and Perri (2012), we have proposed a DC model, which has been implemented with the following aims:

- to improve the accuracy of modeled I-V curves, in particular in the knee and saturation regions;
- to give the device source-drain current as a function of external voltages, as seen at the device gates, by-passing the very difficult measurement of parasitic resistances for the I-V characterization.
- to use empirical parameters to be extracted by a quick and accurate procedure, the initial

estimation of empirical parameters being performed referring to measured I-V curves and to physical considerations, making univocal, fast and easy the extraction of the best fitting parameter set.

An exhaustive description of our DC model is in (Marani and Perri 2012). In this Section we just describe the main equations on which our I-V model is based.

Our DC model, without taking into account the temperature T, has the following expression

$$I_{dss}(V_{ds},V_{gs}) = I_{dss}\left[\left(1-\frac{V_{gs}}{V_t}\right)^N\right]\left[\tanh(\alpha V_{ds})\right]^M \tag{1}$$

where I_{dss} is the maximum saturation drain current, which is not an empirical parameter

$$V_t = V_{to} + \gamma \times V_{ds} \times V_{gs}$$

is the threshold voltage, V_{to} is the threshold voltage at zero bias, γ is the threshold voltage shift parameter, and

$$N = N_0 + N_1 V_{gs} + N_2 V_{gs}^2 + N_3 V_{gs}^3 \tag{2a}$$

$$\text{alpha} = a_0 + a_1 V_{gs} + a_2 V_{gs}^2 + a_3 V_{gs}^3 \tag{2b}$$

being V_{ds} the drain-source voltage and V_{gs} the gate-source voltage.

Eqs. (2) allow the third order dependence of N and α on the bias conditions, improving the fitting in the linear, knee and saturation regions. Moreover, the M parameter improves the fitting in the knee region, modifying here the behavior of hyperbolic tangent function.

The voltages in Eq. (1) are external, i.e., measured at the device external terminals. In this way it is possible to overcome the problem of measurement of the parasitic resistances, thus making easier the parameter extraction procedure and the use of the model for circuit design. If the complete DC device characterization requires the resistances to be determined, the linear approximation can be used for them without affecting the I-V model accuracy.

The extraction of the 11 empirical parameters by an appropriate optimization routine is widely described in our Ref. (Marani and Perri 2012) and therefore the reader is requested to consult it.

In this paper we enhance the previous DC model to simulate accurately the effect of device negative output conductance, especially due to self-heating.

In particular we propose that temperature effects on I-V characteristics can be modeled by the dependence on temperature of the device threshold voltage and of the maximum saturation drain-source current, because of their strong sensitivity to the temperature variations as suggested by the device physical behavior analysis (Perri 2011). In fact internal thermal effects cause mainly a decrease of current in saturation region, that is the output negative differential conductance phenomenon for high gate-source voltage V_{gs}, occurring as a consequence of the reduced mobility and saturation velocity. In correspondence to low V_{gs}, near the threshold voltage, there is an increase of current with temperature. This phenomenon can be modeled as a shift in the threshold voltage, that decreases as the temperature increases (Perri 2011, Marani and Perri 2016).

We propose that temperature effects on I-V characteristics can be modeled by the following equation for drain-source current I_{ds}

$$I_{ds}(V_{ds},V_{gs},T) = I_{dss}(T)\left[\left(1-\frac{V_{gs}}{V_t(T)}\right)^N\right]\left[\tanh(\alpha V_{ds})\right]^M \quad (3)$$

Therefore, in order to evaluate $I_{ds}(V_{ds}, V_{gs}, T)$, it is necessary to determine the dependence of I_{dss} and of V_t on temperature.

As we have already said, firstly, we extract the 11 fitting parameters, i.e., V_{to}, γ, N_o, N_1, N_2, N_3, a_o, a_1, a_2, a_3, M, by minimizing a squared error function within the required tolerance (typically 10^{-4}), at room temperature, according to the procedure described in our Ref. (Marani and Perri 2012), where we have reported the resulting extracted parameters, obtaining also a very good agreement between measured (Javey *et al*. 2002, 2003) and modelled data in terms of I_{ds} versus V_{ds}, with a CPU calculation time very short (0.03 s, by using a 2.4 GHz compatible PC).

In this paper, in order to extract the 2 parameters depending on thermal effects, i.e., V_t and I_{dss} at different temperatures, we propose the following procedure:

(1) we determine the simulated I-V characteristics of the device, obtained by our Eq. (3), in which, at first, we consider the values of V_t and I_{dss} parameters at room temperature;
(2) then we extract the I_{dss} parameters from the simulated I-V output characteristics at considered temperatures and the V_t parameters from the modelled trans-characteristics of the device.

The proposed procedure has been applied also to the numerical model online available (Rahman *et al*. 2006), named FETToy, in order to compare the two considered models.

3. Discussion of results

The simulations were performed at the temperature of 250 K and 500 K in Agilent Technologies CAD ambient, Advanced Design System (ADS). We referred to a CNTFET, whose features are reported in (Naderi *et al*. 2012) to perform our simulations The device has a zig-zag (19,0) CNT structure with approximately 1.5 nm radius which is embedded in cylindrical gate insulator of HfO_2 with the thickness and dielectric constant (k) of 2 nm and 16, respectively. The length of source and drain regions is equal to 20 nm. The channel is intrinsic and its length is 20 nm. There is no overlap between the source (drain) and gate regions.

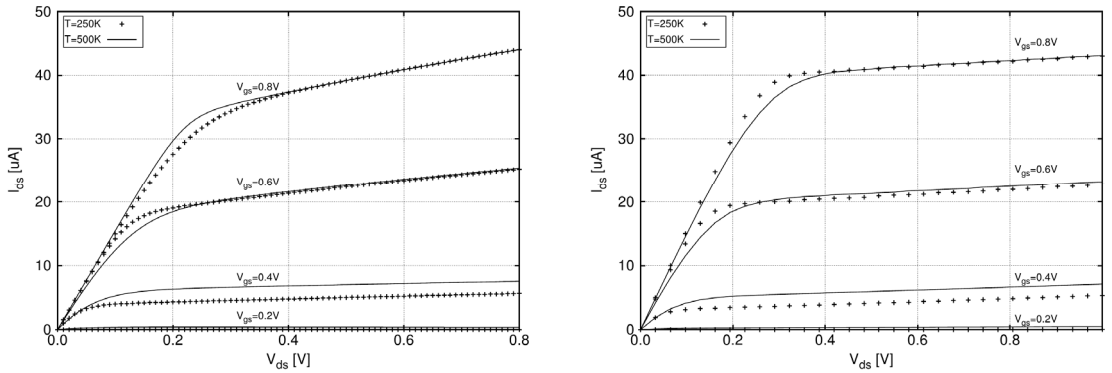
Fig. 1 shows the I-V output characteristics of the two considered models, at various temperatures.

It can be seen from Fig. 1 that for low gate source voltages, at temperature of 500 K, the drain current I_{DS} is higher than that at 250 K. In spite of this, as V_{GS} increases, at low drain source voltages, I_{DS} at 500 K is less than that at 250 K.

In the saturation region, by increasing V_{GS}, the drain current difference between high and low temperature reduces. It is evident from Fig. 1(a) that the drain current in the saturation region and V_{GS} = 0.8 V for 250 K and 500 K are approximately equal. This claim appears to be less verified for the FETToy model for V_{GS} = 0.6 V (Fig. 1(b)).

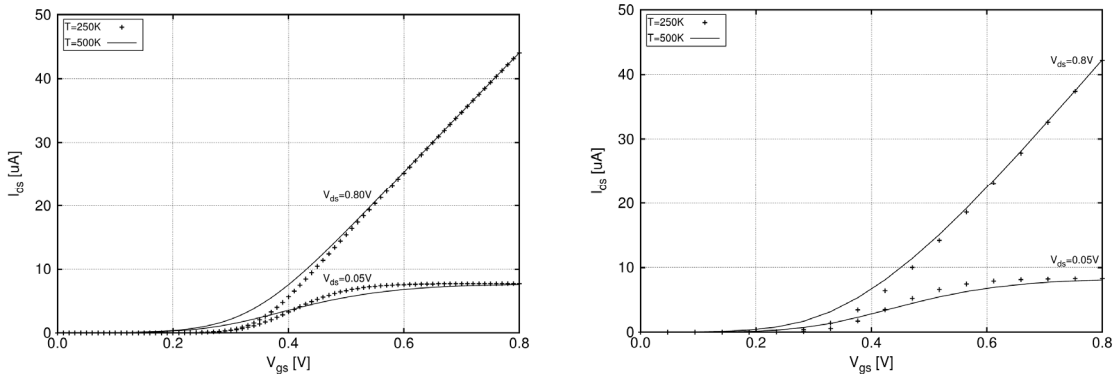
Similarly, Fig. 2 shows the trans-characteristics of the device, obtained by the considered two models.

As it is possible to see from Fig. 2, at V_{DS} = 0.8 V the current raises, when temperature decreases from 500 K to 250 K, while the threshold voltage of the device decreases.



(a) (b)

Fig. 1 I_{DS} versus V_{DS} at different temperatures and different V_{GS} for: (a) proposed model; (b) FETToy model



(a) (b)

Fig. 2 I_{DS} versus V_{GS} at different temperatures and different V_{DS} for: (a) proposed model; (b) FETToy model

Moreover, for $V_{DS} > 0.8$ V, both in our model and in FETToy model the current dependence on temperature is almost zero.

While the current rises with temperature T is present also at $V_{DS} = 0.05$ V for $V_{GS} < 0.4$ V, the dependence is inverted for our and FETToy models for $V_{GS} > 0.4$ V.

According to the proposed procedure, Figs. 1 and 2 allow us to extract respectively the thermal parameters I_{dss} and V_t at considered temperatures (250 K and 500 K).

The obtained results are summarized in Tables 1 and 2 respectively.

In particular in Table 1 we have reported, for both models, the extracted values of current I_{dss} at 250 K and 500 K, for different gate-source voltages, while in Table 2 we have reported the extracted values of threshold voltage of the device at temperatures of 250 K and 500 K with V_{DS} equal to 0.8 V and 0.05 V.

The obtained results show that the values of saturation current for different temperature are equal for high V_{GS} for the proposed model and the FETToy numeric model.

Table 1 Extracted parameter I_{dss} at different temperatures for the two considered models

	Proposed model		FETToy model	
V_{GS}	I_{dss} (at V_{DS} = 0.8 V)		I_{dss} (at V_{DS} = 0.8 V)	
	250 K	500 K	250 K	500 K
0.2 V	10.5 nA	0.365 μA	154 nA	0.416 μA
0.4 V	5.64 μA	7.56 μA	4.84 μA	6.66 μA
0.6 V	25. 2 μA	25.4 μA	22.0 μA	22.5 μA
0.8 V	44.1 μA	44.1 μA	42.2 μA	42.3 μA

Table 2 Extracted parameter V_t at different temperatures for the two considered models

	Proposed Model		FETToy Model	
V_{DS}	V_t		V_t	
	250 K	500 K	250 K	500 K
0.05 V	0.33 V	0.26 V	0.34 V	0.29 V
0.8 V	0.34 V	0.33 V	0.38 V	0.37 V

The simulation results of Table 1 show furthermore that the calculation error is very low, but with our semi-empirical model we have a lower CPU calculation time of about 0.01 s, using a 2.4 GHz compatible PC.

4. Conclusions

In this paper we have taken a semi-empirical model, already proposed by us (Marani and Perri 2012), initially utilized to reproduce the measured I - V characteristic curves at room temperature. Then, to simulate very accurately the effect of device negative output conductance, especially due to self-heating, we have enhanced our DC model, introducing the dependence on temperature of the maximum saturation drain-source current and of the device threshold voltage.

These two parameters have been extracted respectively from the simulated output and trans-characteristics of the device in different temperature conditions.

At last, our results have been compared with those of FETToy model (Rahman *et al*. 2006), obtaining, with reference to I-V characteristics, trends comparable, but with CPU calculation times lower. This result allowed us to assert that the proposed model seems particularly suitable to be implemented in CAD applications.

Actually, for any model, we are introducing the dependence on temperature of energy bandgap. Moreover, as the only experimental data have been measured at 300 K, we are implementing a measurement apparatus to characterize in temperature the CNTFETs behavior, to validate the simulation results with also experimental data, measured at different temperatures.

References

Avouris, Ph., Radosavljević, M. and Wind, S.J. (2005), “Carbon nanotube electronics and optoelectronic”, in

Appl. *Physics of Carbon Nanotubes*: *Fundamentals of Theory*, *Optics and Transport Devices*, eds. S.V. Rotkin & S. Subramone, Berlin Heidelberg, Springer-Verlag, pp. 1-25.

Gelao, G., Marani, R., Diana, R. and Perri, A.G. (2011), "A semi-empirical SPICE model for n-type conventional CNTFETS", *IEEE Trans*. *Nanotechnol*., **10**(3), 506-512.

Gelao, G., Marani, R., Pizzulli, L. and Perri, A.G. (2015a), "A model to improve analysis of CNTFET logic gates in Verilog-A - Part I: static analysis", *Current Nanosci*., **11**(4), 515-526.

Gelao, G., Marani, R., Pizzulli, L. and Perri, A.G. (2015b), "A model to improve analysis of CNTFET logic gates in Verilog-A - Part II: dynamic analysis", *Current Nanosci*., **11**(6), 770-783.

Javey, A., Kim, H., Brink, M., Wang, Q., Ural, A., Guo, J., Mcintyre, P., Mceuen, P., Lundstrom, M. and Dai, M. (2002), "High–Kdielectrics for advanced carbon nanotube transistors and logic gates", *Nature Mater*., **1**, 241-246.

Javey, A., Guo, J., Wang, Q., Lundstrom, M. and Dai, M. (2003), "Ballistic carbon nanotube field-effect transistors", *Nature*, **424**, 654.

Marani, R. and Perri, A.G. (2009), "CNTFET modelling for electronic circuit design", *Electro Chem*. *Transact*., **23**(1), 429 - 437.

Marani, R. and Perri, A.G. (2011), "A compact, semi-empirical model of carbon nanotube field effect transistors oriented to simulation software", *Current Nanosci*., **7**(2), 245-253.

Marani, R. and Perri, A.G. (2012), "A DC model of carbon nanotube field effect transistor for CAD applications", *Int*. *J*. *Electro*., **99**(3), 427 - 444.

Marani, R., Gelao, G. and Perri, A.G. (2012), "Comparison of ABM SPICE library with Verilog-A for compact CNTFET model implementation", *Current Nanosci*., **8**(4), 556-565.

Marani, R., Gelao, G. and Perri, A.G. (2013), "Modeling of carbon nanotube field effect transistors oriented to SPICE software for A/D circuit design", *Microelectro*. *J*., **44**(1), 33-39.

Marani, R. and Perri, A.G. (2016), "A DC thermal model of carbon nanotube field effect transistors for CAD applications", *ECS J*. *Solid State Sci*. *Technol*., **5**(8), M3001-M3004.

Naderi, A., Noorbakhsh, S.M. and Elahipanah, H. (2012), "Temperature dependence of electrical characteristics of carbon nanotube field effect transistors: A quantum simulation study", *J*. *Nanomater*., **2012**, 1-7.

Perri, A.G. (2011), '*Dispositivi Elettronici Avanzat*i', Progedit editor, Bari, Italy.

Rahman, A., Wang, J., Guo, J., Liu, Y., Matsudaira, A., Ahmed, S., Datta, S. and Lundstrom, M. (2006), "FETToy", http://www.nanohub.org

CC