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Quantum modulation of the channel charge and distributed capacitance of double gated nanosize FETs

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Abstract. The structure represents symmetrical metal electrode (gate 1) – front SiO_2 layer – n-Si nanowire FET – buried SiO_2 layer – metal electrode (gate 2). At the symmetrical gate voltages high conductive regions near the gate 1 – front SiO_2 and gate 2 – buried SiO_2 interfaces correspondingly, and low conductive region in the central region of the NW are formed. Possibilities of applications of nanosize FETs at the deep inversion and depletion as a distributed capacitance are demonstrated. Capacity density is an order to $\sim \mu F/cm^2$. The charge density, it distribution and capacity value in the nanowire can be controlled by a small changes in the gate voltages. at the non-symmetrical gate voltages high conductive regions will move to corresponding interfaces and low conductive region will modulate non-symmetrically. In this case source-drain current of the FET will redistributed and change current way. This gives opportunity to investigate surface and bulk transport processes in the nanosize inversion channel.

Keywords: quantization; charge modulation; nanosize FET; capacity

1. Introduction

Capacitors are important components in many integrated circuits. They serve numerous roles in analog and mixed signal circuits, including switched capacitor filters. Capacitors provide a vital role in the decoupling of microprocessors, digital signal processors, and microcontrollers from power supply variations.

The nanotube and nanowire devices can be used as capacitors. In semiconductor nanowires (NW), due to the size quantization, the conductance exhibits quantum effects. It is necessary to take these effects into account in future electronic circuits of nanometer dimensions. It would be also possible to construct new devices with some unique functionality. Note that the ability to control physical properties of semiconducting nanowires has made them attractive devices to study quantum effects at a very small scale. Nanotubes and nanowires dramatically boost the amount of surface, and thus electrical charge, that each metal electrode can possess. The potential for smaller and more powerful capacitors might prove crucial in developing microchips with ever denser circuitry. Moreover, such nanoscale capacitors might help improve the development of compact and cost effective supercapacitors. The nanoscale capacitors might also serve in advanced memory

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chips.

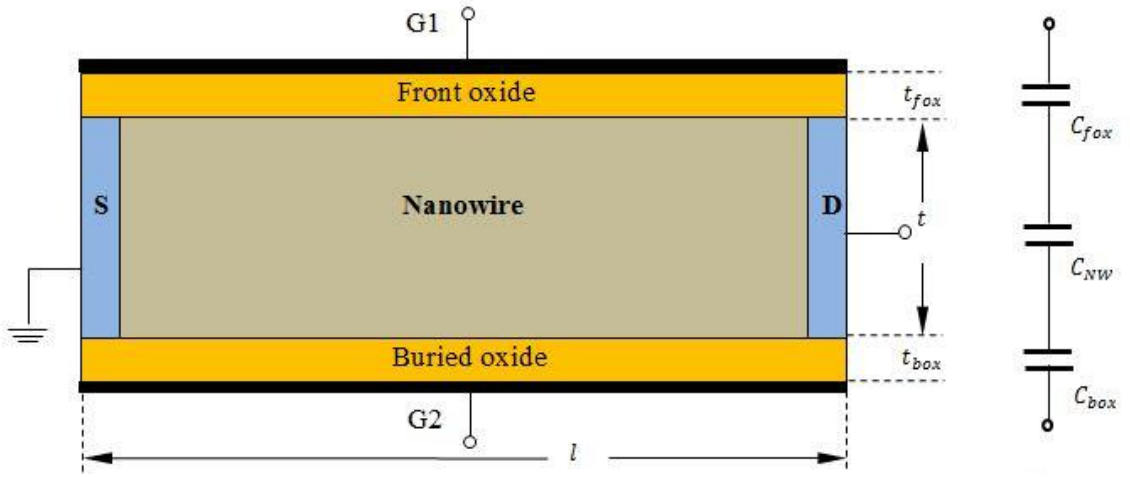
Multi-component nanowire structures in coaxial configuration, such as p-type/intrinsic/n-type silicon nanowire (Tian *et al.* 2007) and metal-insulator-metal (MIM) nanowires (Banerjee *et al.* 2008, Kemell *et al.* 2007, Klootwijk *et al.* 2008, Shelimov *et al.* 2000) have promising applications as fundamental building blocks in future electronic (Tian *et al.* 2007, Kempa *et al.* 2008), photonic (Liu *et al*. 2011), power storage and delivery devices (Banerjee *et al.* 2008, Kemell *et al.* 2007, Klootwijk *et al.* 2008, Shelimov *et al.* 2000). High-density and flexible capacitors are in high demand with the rapid growth of renewable energy industry. Values of MIM micro/nano-capacitors with capacitance densities ranging from 2.5 to 100 μF/cm^2, via depositing alternating metallic and insulating layers inside the anodic aluminum oxide nanopores are reported in (Banerjee *et al.* 2008, Kemell *et al.* 2007, Klootwijk *et al.* 2008, Shelimov *et al.* 2000). Such devices have high power density but low flexibility when integrating with two-dimensional architectures. Whereas a direct growth of similar structures may be much easier to integrate into flexible substrate, micro/nano-electromechanical system (Sazonova *et al.* 2004, Steele *et al.* 2009), lab-on-a-chip device (Daw and Finkelstein 2006) and so on. A single Cu-Cu_2O-C (metal-insulator-carbon) coaxial nanowire capacitor demonstrates also. Cu (inner core) and C (shell) serve as conducting layers and Cu_2O - as an interfacial dielectric layer. The measured capacitance is 10–40 times larger than the value calculated based on a classic cylindered capacitor model. Remarkable capacitance density as high as 143 μF/cm^2 is found for such nanowire capacitors, exceeding previously reported values of MIM micro/nano-capacitors (Banerjee *et al.* 2008, Kemell *et al.* 2007, Klootwijk *et al.* 2008, Shelimov *et al.* 2000). The Cu-Cu_2O-C nanowires also exhibit high electrical conductivity, current-carrying capacity, as well as excellent thermal stability. Quantum mechanical calculations indicate that this unusually high capacitance may be attributed to a negative quantum capacitance of the dielectric–metal interface, enhanced significantly at the nanoscale (Liu *et al.* 2012).

In 1993, electrical conductance quantization was found in gold nanowires made with the scanning tunneling microscope technique at room temperatures (Pascual *et al.* 1993). The electrical models that have been developed for carbon nanotubes for use in the development of a carbon nanotube capacitor model are reviews in Refs. (Budnik *et al.* 2009a, b).

Note that the local charge concentration and hence the conductance of the nanowires was quite sensitive to small changes of the gate voltage.

2. Nanowire capacitance behavior

Nanosized FETs are the main active parts for lot of nanosized bio- and chemical sensors and other sensitive devices. The schematic picture of the investigated structure is presented on Fig. 1. The structure represents symmetrical metal electrode (gate 1, G1) -front oxide (fox) layer - NW - buried oxide (box) layer - metal electrode (gate 2, G2). Nanowire has n-type conductivity Si, fox and box are SiO_2 layers having the same sizes. It can be regulated source-drain current in the lateral NW FET by the changing gate voltages. We take the simple case of equality of gate voltages $|V_{g1}| = |V_{g2}|$ for physical explaining and numerical estimation in further. Source of the lateral FET connected on ground. After applying gate voltages within in the NW near the fox and box layers the deep accumulation (inversion) and depletion layers can be formed, correspondingly. As it is known, size quantization effect appears in the inversion layer of NW FETs (Pud *et al.* 2014) that brings to specific redistribution of the charge carriers inside NW. In the quantum case, a



(a) (b)

Fig. 1 Schematic picture (a) and equivalent capacitive scheme (b) of the investigated structure. S and D are source and drain, t, t_{fox} and t_{box} are thicknesses of the NW, fox and box layers, correspondingly, l is the length of NW

conception of the uniform inversion layer approximation becomes inappropriate. Recently we show that in the case switch off back gate (G2) voltage, the growth of the G1 gate voltage $(V_{g1} > 0)$ results in an increase in the maximal concentration of electrons and also in a shift of its maximum towards the fox-nSi NW interface (see Fig. 5(b) in (Pud *et al.* 2014)). The majority of the electrons is located near fox layer and occupies the region at a depth of 1-2 nm. The maximum of electron concentration moves away from the interface into the depths of the NW depending on applied gate voltage. In the case of the switch on both front and back gate voltages $(|V_{g1}| = |V_{g2}|;\ V_{g2} < 0)$ in the NW near the box deep depletion region is formed. This positive charge region is conditioned by the ionized donor atoms in the NW. In this case maximal value of the positive charge shifts towards the box-NW interface. Such distributions plotted on the base of the expressions (15), (4), (7) of Ref. (Pud *et al.* 2014) and using same electro-physical and geometrical parameters of oxide layers and NW (we take equality of the fox and box layer's thicknesses $t_{fox} = t_{box} = 10$ nm) present on Fig. 2.

It is clear that regulation of the low conductive region width will be more effective for the small thickness NW. In this case by the small changing of the gate voltages (V_{g1} and V_{g2}) we can effectively cover low conductive region. Voltage-dependent capacitance density C_{NW} can be defined as follows

$$C_{NW}(V_g) = \frac{dQ(x,V_g)}{dV_g}. \tag{1}$$

Here Q is the charge density of the high conductive region that is equal to

$$Q(x,V_g) = \frac{eN}{A} = \frac{e\Omega n(x,V_g)}{A} = \frac{elwt'n(x,V_g)}{lw} = et'n(x,V_g), \tag{2}$$

where e is the elementary charge, N is the total number of electrons, $n(x,V_g)$ is the electron

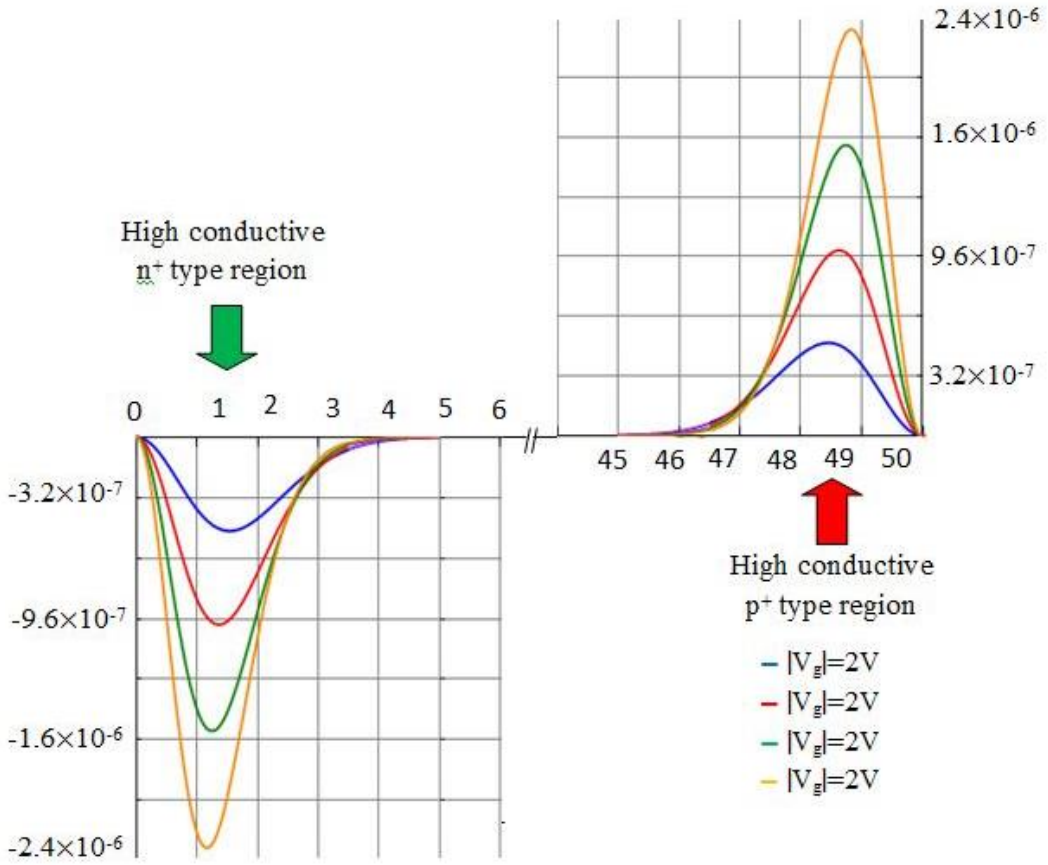


Fig. 2 Distribution of the charge density in the n-SiNW having $t' \approx 2$ nm average effective thickness in the case $|V_{g1}| = |V_{g2}| \equiv |V_g|$

concentration depending on coordinate x and gate voltage, $A = wl$ is the capacitor plate area, Ω is the volume and t' is the effective thickness of the high conductive region, correspondingly, x is the coordinate on the direction from fox/box-NW interface.

Substituting Eq. (2) into Eq. (1) we have

$$C_{NW}(V_g) = et' \times \frac{dn(x,V_g)}{dV_g}. \tag{3}$$

The position of the maximal concentration of electrons x_m depends on gate voltage as follows (see Fig. 10 in Pud *et al.* (2014))

$$x_m \approx 1.21 + 1.64 \times exp(-0.88V_g) \text{ nm}. \tag{4}$$

Using the value at the electron maximum concentration $x = x_m$, we can define the maximal value of capacitance density $C_{NW}(V_g)_m$

$$C_{NW}(V_g)_m \approx et' \times \frac{n(x_m,V_g)}{V_g} = \frac{Q_m}{V_g}. \tag{3a}$$

Here Q_m is the maximal charge density of the high conductive region. On the Fig. 2 electrical charge distribution in the accumulation/inversion and depletion layers near the fox-NW and box-NW interfaces are presented for the several values of the applied gate voltages. Those dependencies plotted using corresponding expressions and same data which we use in (Pud *et al.* 2014). Near the fox and box layers high conductive regions are formed. Between the two high conductive regions (as a capacitor plates) and low conductive central region (as an insulator) capacitance C_{NW} is formed (see Fig. 2, Fig. 1(b)). It is distributed capacitance.

Total measurable capacitance C between electrodes G1 and G2 is equal to

$$\frac{1}{C} = \frac{1}{C_{fox}} + \frac{1}{C_{NW}} + \frac{1}{C_{box}} \quad . \tag{5}$$

Here C_{fox} and C_{box} are capacitances of the fox and box layers, correspondingly

$$C_{fox/box} = \frac{\varepsilon\varepsilon_0}{t_{fox/box}} . \tag{6}$$

Here ε and $\varepsilon_0 = 8.85 \times 10^{-14}$ F/cm are the dielectric permittivity of silicon dioxide and free space, correspondingly.

We can estimate maximal values of the capacitance densities from data of Fig. 2 and Eqs. (3a), (5) and (6). They are: $C_{NW} = 0.24$ μF/cm^2 ($|V_{g1}| = |V_{g2}| = 2$ V) and 0.45 μF/cm^2 ($|V_{g1}| = |V_{g2}| = 5$ V), $C_{fox} = C_{box} = 3.4515\,\mu$F/cm^2. Finally for our case: $C \approx 0.2$ μF/cm^2 at the $|V_{g1}| = |V_{g2}| = 2$ V and $C \approx 0.4$ μF/cm^2 at the $|V_{g1}| = |V_{g2}| = 5$ V.

3. Conclusions

We demonstrate the possibility of the application of the nanosize FETs at the deep accumulation/inversion and depletion as a regulated distributed capacitance. Without any special constructions and new additions it can be achieved capacity value an order to ~μF. Those values are smaller as compared with reference data for nanosized MIMs and metal-insulator-carbon capacitors. They can be have special promising applications in the field of nanosized electronics, bio-electronics, medicine, as fundamental building blocks in future electronic, photonic, power storage and delivery devices.

Note that at the non-symmetrical gate voltages when $|V_{G1}| \neq |V_{G2}|$ high conductive regions will move to corresponding interfaces and low conductive region will modulate non-symmetrically. In this case source-drain current will redistributed and change current way. This gives opportunity to investigate surface and bulk transport processes in the nanosize inversion channel. In near future electronic circuits of nanometer dimensions it would be necessary to take this effect into account and it would be also possible to construct new devices with some unique functionality. Investigation of the peculiarities of the nanosized capacitors made them attractive devices to study quantum effects at a very small scale.

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