Quantum modulation of the channel charge and distributed capacitance of double gated nanosize FETs

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Abstract. The structure represents symmetrical metal electrode (gate 1) – front SiO_2 layer – n-Si nanowire FET – buried SiO_2 layer – metal electrode (gate 2). At the symmetrical gate voltages high conductive regions near the gate 1 – front SiO_2 and gate 2 – buried SiO_2 interfaces correspondingly, and low conductive region in the central region of the NW are formed. Possibilities of applications of nanosize FETs at the deep inversion and depletion as a distributed capacitance are demonstrated. Capacity density is an order to $\sim \mu F/cm^2$. The charge density, it distribution and capacity value in the nanowire can be controlled by a small changes in the gate voltages. at the non-symmetrical gate voltages high conductive regions will move to corresponding interfaces and low conductive region will modulate non-symmetrically. In this case source-drain current of the FET will redistributed and change current way. This gives opportunity to investigate surface and bulk transport processes in the nanosize inversion channel.

Keywords: quantization; charge modulation; nanosize FET; capacity

1. Introduction

Capacitors are important components in many integrated circuits. They serve numerous roles in analog and mixed signal circuits, including switched capacitor filters. Capacitors provide a vital role in the decoupling of microprocessors, digital signal processors, and microcontrollers from power supply variations.

The nanotube and nanowire devices can be used as capacitors. In semiconductor nanowires (NW), due to the size quantization, the conductance exhibits quantum effects. It is necessary to take these effects into account in future electronic circuits of nanometer dimensions. It would be also possible to construct new devices with some unique functionality. Note that the ability to control physical properties of semiconducting nanowires has made them attractive devices to study quantum effects at a very small scale. Nanotubes and nanowires dramatically boost the amount of surface, and thus electrical charge, that each metal electrode can possess. The potential for smaller and more powerful capacitors might prove crucial in developing microchips with ever denser circuitry. Moreover, such nanoscale capacitors might help improve the development of compact and cost effective supercapacitors. The nanoscale capacitors might also serve in advanced memory

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chips.

Multi-component nanowire structures in coaxial configuration, such as p-type/intrinsic/n-type silicon nanowire (Tian *et al.* 2007) and metal-insulator-metal (MIM) nanowires (Banerjee *et al.* 2008, Kemell *et al.* 2007, Klootwijk *et al.* 2008, Shelimov *et al.* 2000) have promising applications as fundamental building blocks in future electronic (Tian *et al.* 2007, Kempa *et al.* 2008), photonic (Liu *et al*. 2011), power storage and delivery devices (Banerjee *et al.* 2008, Kemell *et al.* 2007, Klootwijk *et al.* 2008, Shelimov *et al.* 2000). High-density and flexible capacitors are in high demand with the rapid growth of renewable energy industry. Values of MIM micro/nano-capacitors with capacitance densities ranging from 2.5 to 100 $\mu F/cm^2$, via depositing alternating metallic and insulating layers inside the anodic aluminum oxide nanopores are reported in (Banerjee *et al.* 2008, Kemell *et al.* 2007, Klootwijk *et al.* 2008, Shelimov *et al.* 2000). Such devices have high power density but low flexibility when integrating with two-dimensional architectures. Whereas a direct growth of similar structures may be much easier to integrate into flexible substrate, micro/nano-electromechanical system (Sazonova *et al.* 2004, Steele *et al.* 2009), lab-on-a-chip device (Daw and Finkelstein 2006) and so on. A single Cu-Cu_2O-C (metal-insulator-carbon) coaxial nanowire capacitor demonstrates also. Cu (inner core) and C (shell) serve as conducting layers and Cu_2O - as an interfacial dielectric layer. The measured capacitance is 10–40 times larger than the value calculated based on a classic cylindered capacitor model. Remarkable capacitance density as high as 143 $\mu F/cm^2$ is found for such nanowire capacitors, exceeding previously reported values of MIM micro/nano-capacitors (Banerjee *et al.* 2008, Kemell *et al.* 2007, Klootwijk *et al.* 2008, Shelimov *et al.* 2000). The Cu-Cu_2O-C nanowires also exhibit high electrical conductivity, current-carrying capacity, as well as excellent thermal stability. Quantum mechanical calculations indicate that this unusually high capacitance may be attributed to a negative quantum capacitance of the dielectric–metal interface, enhanced significantly at the nanoscale (Liu *et al.* 2012).

In 1993, electrical conductance quantization was found in gold nanowires made with the scanning tunneling microscope technique at room temperatures (Pascual *et al.* 1993). The electrical models that have been developed for carbon nanotubes for use in the development of a carbon nanotube capacitor model are reviews in Refs. (Budnik *et al.* 2009a, b).

Note that the local charge concentration and hence the conductance of the nanowires was quite sensitive to small changes of the gate voltage.

2. Nanowire capacitance behavior

Nanosized FETs are the main active parts for lot of nanosized bio- and chemical sensors and other sensitive devices. The schematic picture of the investigated structure is presented on Fig. 1. The structure represents symmetrical metal electrode (gate 1, G1) -front oxide (fox) layer - NW - buried oxide (box) layer - metal electrode (gate 2, G2). Nanowire has n-type conductivity Si, fox and box are SiO_2 layers having the same sizes. It can be regulated source-drain current in the lateral NW FET by the changing gate voltages. We take the simple case of equality of gate voltages $|V_{g1}| = |V_{g2}|$ for physical explaining and numerical estimation in further. Source of the lateral FET connected on ground. After applying gate voltages within in the NW near the fox and box layers the deep accumulation (inversion) and depletion layers can be formed, correspondingly. As it is known, size quantization effect appears in the inversion layer of NW FETs (Pud *et al.* 2014) that brings to specific redistribution of the charge carriers inside NW. In the quantum case, a