Advances in Materials Research, Vol. 1, No. 2 (2012) 109-113
DOI: http://dx.doi.org/10.12989/amr.2012.1.2.109

Electromigration-induced void evolution in upper and lower layer dual-inlaid Copper interconnect structures

D.J. Pete*[1], S.G. Mhaisalkar[2], J.B. Helonde[3] and A.V. Vairagar[4]

[1]*Datta Meghe College of Engineering, Navi Mumbai, India*
[2]*School of Materials Engineering, Nanyang Technological University, Singapore*
[3]*ITM College of Engineering, Nagpur, India*
[4]*OMScientific Private Limited, Pune, India*

(Received November 10, 2011, Revised March 26, 2012, Accepted May 26, 2012)

Abstract. Electromigration-induced void evolutions in typical upper and lower layer dual-inlaid Copper (Cu) interconnect structures were simulated by applying a phenomenological model resorting to Monte Carlo based simulations, which considers redistribution of heterogeneously nucleated voids and/or pre-existing vacancy clusters at the Copper/dielectric cap interface during electromigration. The results indicate that this model can qualitatively explain the electromigration-induced void evolutions observations in many studies reported by several researchers heretofore. These findings warrant need to re-investigate technologically important electromigration mechanisms by developing rigorous models based on similar concepts.

Keywords: electromigration in Copper; surface void migration; dual-inlaid Copper interconnect

1. Introduction

Electromigration (EM) continues to be one of the most important reliability issues in integrated circuit (IC) interconnects. In Copper (Cu) interconnect structures, which replaced earlier Aluminium (Al) interconnects, EM is being intensively studied because of its immense technological importance. However, the mechanism of EM-induced void evolution in conventional dual-inlaid Cu interconnect structures is not completely understood.

For most of the dual-damascene processes and structured manufactured currently, the interfacial diffusion at the copper/silicon nitride (Cu/ SiN_x) interface adversely affects the EM lifetime in Cu interconnects as opposed to grain boundary diffusion in Al alloy conductors, reported by Meyer *et al.* (2002), Vairagar *et al.* (2004). I*n-situ* scanning electron microscopy (SEM) observations by many researchers Vairagar *et al.* (2005), Gan *et al.* (2001, 2002), of upper and lower layer dual-damascene structures indicated that voids nucleate heterogeneously at the Cu/SiN_x interface at locations far away from the cathode, move along the Cu/SiN_x interface in opposite direction of electron flow (it is a virtual movement since actually copper atoms are transported in the opposite direction), and eventually agglomerate at the cathode end above the via prior to subsequent growth leading to eventual failure at the via, reported by Gan *et al.* (2003).

*Corresponding author, Research Scholar, E-mail: pethedj@rediffmail.com

While the *in-situ* SEM observation provides a direct evidence of void migration behaviour, analytical, numerical or Monte Carlo simulations are necessary for further understanding the underlying physical mechanisms. The utmost objective is to generate some design guidelines for EM resistant circuits. In this paper, the void shape evolution behaviour of the EM-induced void migration in Cu dual-damascene interconnects were investigated through Monte Carlo simulation.

Time-dependent EM-induced voiding mechanisms in Cu in-laid structures were revealed by our previous *in-situ* SEM studies (Meyer *et al.* 2002, Vairagar *et al.* 2004, 2005). However, these peculiar void evolutions could not be completely explained by the conventional theory of maximum tensile stress developed at the cathode flux divergence site (Vairagar *et al.* 2004, 2005, Gan *et al*. 2001, 2002).

2. Model and assumption

In this paper, a phenomenological model is proposed to explain these EM-induced voiding observations as follows:

Heterogeneously nucleated EM-induced voids and/or pre-existing vacancy clusters at the Cu/dielectric cap interface are assumed, which represent small pre-existing voids/vacancy clusters at the Cu/dielectric cap interface due to damage during chemical mechanical polishing (CMP) and dielectric cap deposition in Cu interconnects. These voids and/or pre-existing vacancy clusters are redistributed at the Cu/dielectric cap interface as a consequence of a directed atomic transport during EM process. This redistribution takes place along the entire length of the interconnect leading to void formation at Cu/dielectric cap interface in the cathode region.

The voids migrate virtually (actually it is an atomic transport into the opposite direction) along the Cu/dielectric cap interface in a direction opposite to electron flow and eventually agglomerate at the cathode end. No significant change in the resistance of the copper interconnect structure is observed in typical electromigration test until this point, although void evolution takes place in the cathode region. Significant agglomeration and evolution of voids takes place at the cathode end of the interconnect structure, which leads eventually to failure.

3. Simulation

A simple model was implemented using random atomic jumps based on the Monte Carlo method to simulate redistribution of voids/vacancy clusters due to electromigration. A simplified 2-dimensional version of Monte-Carlo simulation approach was used for the present study. Only two parameters were considered - electron wind force and bonding energy.

Monte Carlo scheme is governed by calculation of change of energies for deciding success of an atomic jump between randomly selected neighboring atomic positions. A simplified metropolis Monte Carlo algorithm was employed in which atomic jump was successful only for reduction in energy. Energy consists of sum of pair interaction energies N^*Eb (N-number of filled neighboring sites, $0 \leq N \leq 8$, Eb- binding energy per link) and of effective electric energy due to the electron wind force. We introduced a lower interaction energy at the surface of interconnect line to simulate weak Cu/dielectric cap interface conditions at this surface. Complete code for the simulations was written in MatLab. A square lattice is employed for ease in programming and atomic jumps to eight neighboring atomic positions are considered. For random selection of atoms, only an atomic

position with at least one neighboring vacancy was considered to save computational time. Pair interaction energies were re-calculated only after atom jump between an atomic location filled with an atom and a location with a vacancy. The force due to electron wind force was simulated by introducing a linear force gradient from one end of the line to another. The interaction energy was considered to be relatively higher than the gradient due to the electromigration wind force.

Similar Monte Carlo-based by Mehl *et al.* (2000), Bruschi *et al.* (2000), Rous *et al*. (2001) as well as finite element method-based models, by Bhate *et al*. (2000) were reported previously to study electromigration-induced void evolution. However, such approaches have not been extensively used for investigation of electromigration void evolutions in various dual in-laid Cu interconnect structures, perhaps due to lack of direct and detailed experimental evidence of exact void evolution during electromigration stressing. Now, considering the results from recently published *in-situ* SEM electromigration studies, by Meyer *et al.* (2002), Vairagar *et al.* (2004) an attempt is made in the present study to do so.

In-situ electromigration studies provided detailed information on exactly how void evolution takes place in different dual-inlaid Cu interconnect structures. Electromigration-induced void movement along the Cu/SiN_x interface in a direction opposite to the electron flow was observed in all test structures during *in-situ* characterizations (Meyer *et al*. 2002, Vairagar *et al*. 2004, 2005). The general observation of the void migration mechanism is simulated in this study. Furthermore, void evolution at cathode via region in lower and upper layer test structure was simulated.

4. Results and discussion

Electromigration in Cu interconnects was simulated with the initial condition of pre-existing vacancy clusters at the Cu/dielectric cap interface as shown in Fig. 1. The results indicated that initial vacancy clusters will remain at the Cu/dielectric-cap interface, vacancies will be captured at this interface and virtually move in a direction opposite to electron flow. Note that this was a simulation of a region along the Cu/dielectric interface, which was only a small section out of the whole interconnect line. However, this phenomenon will occur throughout the entire length of the Cu interconnect line. It can

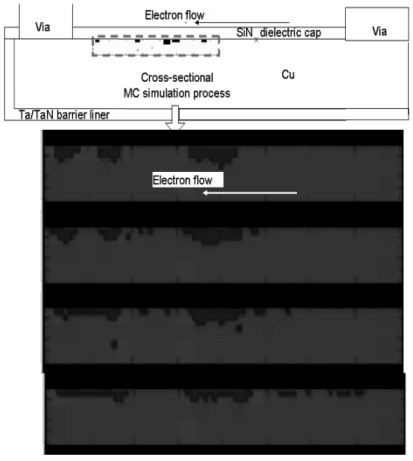

Fig. 1 Simulation of vacancies captured at surface and void movement opposite to electron flow

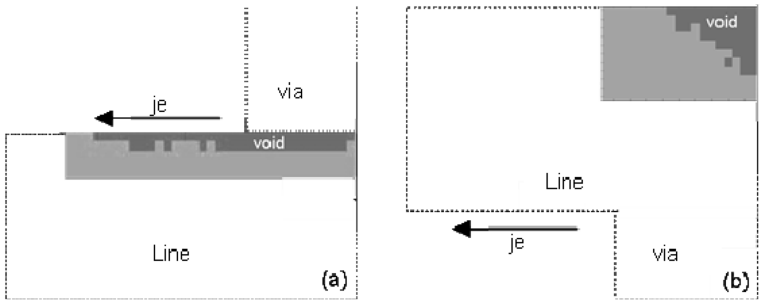

Fig. 2 Simulation of void agglomeration at cathode via region of (a) lower layer test structure and (b) upper layer test structure

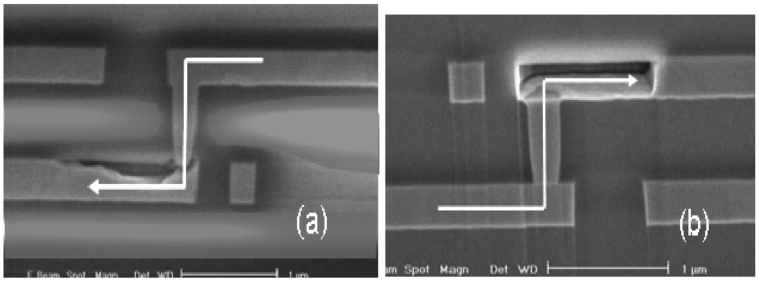

Fig. 3 Peculiar EM-induced voiding in Cu interconnect structures revealed by *in-situ* SEM studies: (a) cathode-end via in lower layer structure and (b) in upper layer structure (Meyer *et al*. 2002, Vairagar *et al.* 2004)

be inferred that these vacancy clusters will move along the Cu/dielectric cap interface in a direction opposite to electron flow direction leading to agglomeration and eventually void nucleation at the Cu/dielectric-cap interface at the cathode region. This observation is consistent with *in-situ* SEM observations of voids only at the Cu/dielectric cap interface at the cathode end of the interconnect structure reported by Vairagar *et al.* (2004, 2005) and preferential void nucleation at Cu/dielectric cap interface reported in Cu electromigration studies by many researchers Gan *et al*. (2002, 2003, 2004). Further simulations were carried out to replicate electromigration stressing condition in lower and upper layer dual-inlaid Cu interconnect structures with the initial condition of voids along the Cu/dielectric cap interface in the cathode region. Simulation results for void evolution at the cathode via in the lower and upper layer dual-inlaid test structures is shown in Figs. 2(a) and (b) respectively. The void location and shape predicted by the simulation results are similar to the void evolution observed during the initial stage of electromigration degradation by *in-situ* SEM studies Figs. 3(a) and (b) reported by Vairagar *et al*. (2004). These results are also consistent with failure analysis results reported in electromigration studies on similar interconnect structures by other researchers (Gan *et al*. (2001), Fischer *et al*. (2002), Yokogawa *et al*. (2001)).

5. Conclusions

The proposed model can qualitatively explain the peculiar electromigration-induced void movement

observed during experimental *in-situ* SEM characterizations of typical lower and upper layer Cu dual-inlaid interconnect structures as well as in various other reported electromigration studies. These peculiar void evolutions could not have been discerned by the conventional theory of void nucleation and growth at maximum tensile stress at the cathode flux divergence site. However, this model is relatively simple and it provides only qualitative explanation of void evolution during the initial stage of electromigration, well before any resistance change is detected. These findings warrant need to re-investigate technologically important electromigration mechanisms such as the reservoir effect and the short-length effect by developing rigorous physically based model based on similar concepts, considering other important parameters such as stress and temperature gradients, current density distribution, microstructure and introducing diffusivities for different atomic transport paths. Such approaches will provide quantitative information and further in-depth understating of electromigration-induced voiding in Cu in-laid interconnect structures.

References

Bhate, D.N., Kumar, A. and Bower, A.F. (2000), "Diffuse interface model for electromigration and stress voiding", *J. Appl. Phys*., **87**(4), 1712-1721.

Bruschi, P., Nannini, A. and Piotto, M. (2000), "Three-dimensional Monte Carlo simulations of electromigration in polycrystalline thin films", *Comp. Mater. Sci.,* **17**(2-4), 299-304.

Fischer, A.H., von Glasow, A., Penka, S. and Ungar, F. (2002), "Electromigration failure mechanism studies on copper interconnects", *Proceedings of IEEE International Interconnect Technology Conference*, 139-141.

Gan, C.L., Thompson, C.V., Pey, K.L., Choi, W.K., Wei, F., B., Yu and Hau-Riege, S.P. (2002), "Experimental characterization of the reliability of 3-terminal dual-damascene copper interconnect trees", *Proceedings of Material Res. Soc. Symp*., 716-431.

Gan, C.L., Thompson, C.V., Pey, K.L. and Choi, W.K. (2003), "Experimental characterization and modeling of the reliability of three-terminal dual-damascene Cu interconnect trees", *J. Appl. Phys*., **94**(2), 1222-1228.

Gan, C.L., Thompson, C.V., Pey, K.L., Choi, W.K., Tay, H.L., Yu, B. and Radhakrishnan, M.K. (2001), "Effect of current direction on the lifetime of different levels of Cu dual-damascene metallization", *Appl. Phys. Lett*., **79**(27), 4592-4595.

Mehl, H., Biham, O., Millo, O. and Karimi, M. (2000), "Electromigration-induced flow of islands and voids on the Cu (001) surface", *Phys. Rev. B*, **61**, 4975-4982.

Meyer, M.A., Langer, E. and Zschech, E. (2002), "In situ SEM observation of electromigration phenomena in fully embedded copper interconnect structures", *Microelectron. Eng.*, **64**(1-4), 375-382.

Rous, P.J. (2001), "Theory of surface electromigration on heterogeneous metal surfaces", *Appl. Surf. Sci*., **175-176**(1-2), 212-217.

Vairagar, A.V., Mhaisalkar, S.G., Krishnamoorthy, A., Tu, K.N., Gusak, A.M., Meyer, M.A. and Zschech, E. (2004), "In situ observation of electromigration-induced void migration in dual-damascene Cu interconnect structures", *Appl. Phys. Lett*., **85**(13), 2502-2504.

Vairagar, A.V., Mhaisalkar, S.G., Meyer, M.A., Zschech, E., Krishnamoorthy, A., Tu, K.N. and Gusak, A.M. (2005), "Direct evidence of electromigration failure mechanism in dual-damascene Cu interconnect tree structures", *Appl. Phys. Lett*., **87**(8), 1063-1065.

Yokogawa, S., Okada, N., Kakuhara, Y. and Takizawa, H. (2001), "Electromigration performance of multi-level damascene copper interconnects", *J. Microelectron. Reliab.*, **41**(9-10), 1409-1416.

Zaporozhets, T.V., Gusak, A.M., Tu, K.N. and Mhaisalkar, S.G. (2005), "Three-dimensional simulation of void migration at the interface between thin metallic film and dielectric under electromigration", *J. Appl. Phys*., **98**(10), 3508-3517.

Zschech, E., Engelmann, H.J., Meyer, M.A., Kahlert, V., Vairagar, A.V., Mhaisalkar, S.G., Ahila, K., Yan, M.Y., Tu, K.N. and Sukharev, V. (2005), "Effect of interface strength on electromigration- induced inlaid copper interconnect degradation : Experiment and simulation", *Z. Metallkd*., **96**, 966-971.